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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,910	01/03/2001	Odutola Oluseye Ewedemi	M-9129 US	5038

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PATENT LAW GROUP LLP
2635 NORTH FIRST STREET
SUITE 223
SAN JOSE, CA 95134

EXAMINER	
WILSON, JACQUELINE B	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,910	EWEDEMI ET AL.	
	Examiner	Art Unit	
	Jacqueline Wilson	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1, 5, 9, 13, 14, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsieh et al. (US 6,757,019).**

Regarding Claim 1, Hsieh et al teaches a sensor array (fig. 4, 22) that outputs digital signals (col. 5, lines 1-8), a data memory (30), and a logic circuit (referred to as processors 40) providing a memory interface (referred to as DMA 50) for exporting pixel data.

Claim 5 is analyzed and discussed with respect to Claim 1, with the further limitation of an analog-to-digital converter coupled to the pixel array for converting the analog signals into digital pixel data. However, Hsieh et al teaches A/D converter coupled to the pixels for converting data to digital signals (col. 5, lines 4+).

Claim 9 is analyzed and discussed with respect to Claim 1. (See rejection of Claim 1 above.)

Regarding Claim 13, Hsieh et al teaches a sensor array (fig. 4, 22) that outputs digital signals (col. 5, lines 1-8), and a dual-port data memory (30). Hsieh et al teaches that the image signals are input into the memory (30) for storage (first port) and a second port which inherently interfaces with other devices for exporting pixel data (to the processors 40). Hsieh et al teaches that the dual-port memory is fabricated with the sensor array on a same integrated chip (col. 1, lines 9+).

Regarding Claim 14, Hsieh et al teaches an image sensor (20) comprising a sensor array (22) that outputs digital signals (col. 5, lines 1-8), a data memory (30), a logic circuit coupled to the data memory (40) and fabricated with the data memory on the same integrated chip (see fig. 4), the logic circuit providing a memory interface (referred to as DMA 50) for exporting pixel data, and an image processing device (also 40) including a memory interface port (50), wherein the image sensor is coupled to the memory interface port of the image processing device (via 30 and 50) and the image processing device accesses pixel data in the image sensor using a memory interface protocol (inherent since the memory operates using a specific frequency and outputs data with a protocol equivalent to the type of memory used).

Claim 18 is analyzed and discussed with respect to Claim 14. (See rejection of Claim 14 above.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 6-8, 10-12, 15-17, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsieh et al in view of Shepherd et al (US 6,434,665).

Regarding Claims 2-4, Hsieh et al fails to specifically disclose the memory interface is a SRAM, DRAM or a packet protocol synchronous DRAM interface. However Shepherd et al teaches it is well known in the art to have memory interfaces able to convert between different frequencies (col. 3, lines 49+). Shepherd et al discloses a memory interface (120) that transfers data from a memory cache subsystem (136) to an external memory (108). These two memory locations operate at different frequencies (depending on whether the memory is SRAM, SDRAM or DRAM; col. 3, lines 34+) in which the bus transfers data. The memory interface is capable of converting the frequency of the data to the desired frequency of the target location for the purpose of properly storing data. Therefore, it would have been obvious to use the teaching of Shepherd et al in the device of Hsieh et al for converting the image data into the proper protocol according to the receiving location (such as using a SRAM or DRAM or packet protocol synchronous DRAM interface).

Claims 6-8, 10-12, 15-17, and 19-21 are analyzed and discussed with respect to Claim 2-4. (See rejection of Claims 2-4 above.)

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacqueline Wilson whose telephone number is (703) 308-5080. The examiner can normally be reached on 8:30am-5:00pm (alternate Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JBW
07/15/04

AUNG MOE
PRIMARY EXAMINER